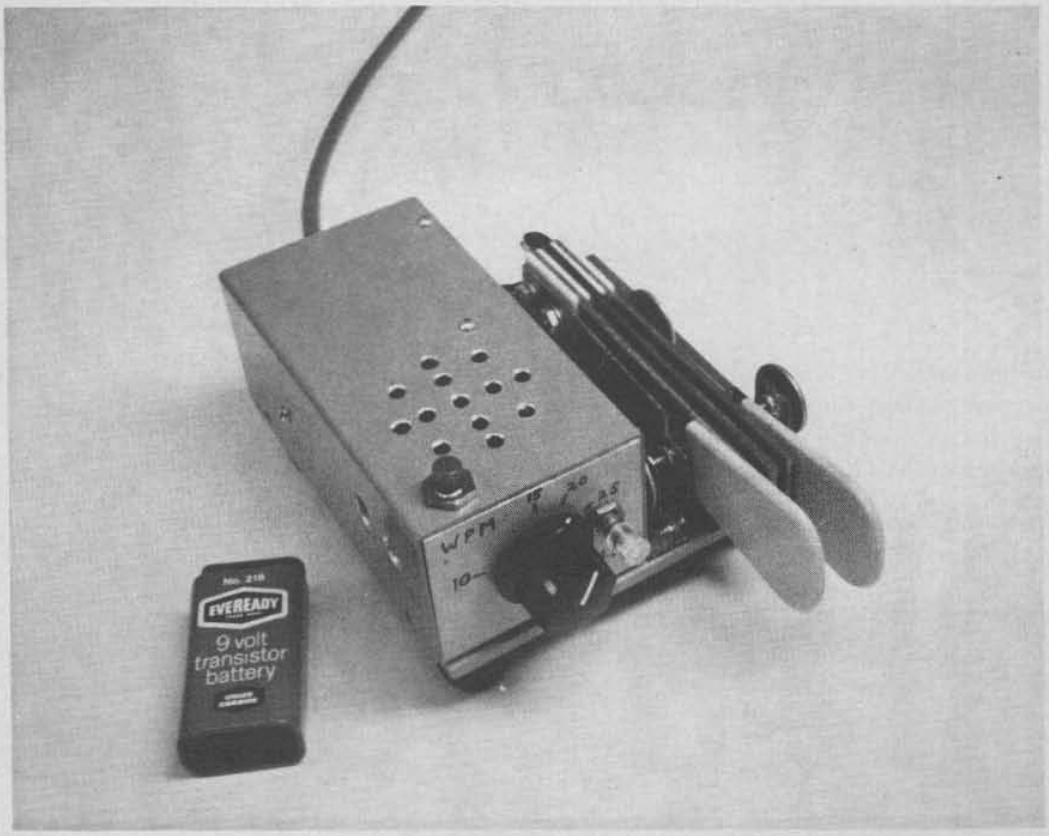


Fig. 1. MINI-MOS electronic keyer with dual paddle key. The transistor battery in the foreground not only shows the size of the keyer, but can also power the keyer for over one year of daily operation.

MINI-MOS--
The Best Keyer Yet?

--nothing Mickey Mouse about this one

Erich A. Pfeiffer WA6EGY
16526 Buchet Drive
Granada Hills CA 91344

Some time ago, when my code speed had gradually crept up to 16 wpm, I felt ready to trade my straight key for something more advanced. A "COSMOS IC electronic keyer," described in an article by WB2DFA[1] seemed to be a good choice. The keyer was built and seemed to perform fine. In due time, however, some limitations were found, which unfortunately proved to be inherent to the design approach chosen by WB2DFA:

- The keyer did not have a dot memory. This makes it necessary to move the keyer paddle exactly in the right rhythm; otherwise one can easily lose dots, especially in letters like K, C and Y.
- The keyer used a continuously running clock. When the dot or dash contact is closed, the keyer has to wait for the next clock pulse before the code element is sent. This is especially noticeable at low code speeds.
- The keyer drew very little current and was, therefore, operated from a 9 volt transistor battery. Theoretically the battery should give over 200 hours of operation. If one forgets to turn off the keyer, however, it does not last very long.

At a local hamfest I had a chance to compare several commercially manufactured keyers, including some that had dot and dash memory and iambic keying. After this experience I was no longer satisfied with my old keyer and decided to design a better one. My keyer was to incorporate the features available

in the best commercial keyers, but would also fully utilize the advantages of complementary MOS technology.

The result of this design project was the MINI-MOS keyer shown in Fig. 1, which has now been in use for over one year. This keyer has the following features:

- Dot and dash memory and gated clock.
- Iambic operation when used with a double ("squeeze") paddle.
- Extremely low standby current, which makes it unnecessary to provide an on-off switch.
- Low "key down" current, which makes it possible to operate the keyer from a normal 9 volt transistor battery for at least one year.
- Low component count (7 ICs and few discrete components).
- Built-in sidetone oscillator with speaker and keying circuit for grid-block keyed transmitter.

The completed keyer is very compact and can be packaged in a minibox measuring only 2 by 2 by 4 inches, including batteries and sidetone speaker. Together with a small dual paddle, the keyer was mounted on a base only 4 by 4 inches in size.

Circuit Description

The keyer utilizes the "complementary metal oxide silicon" or CMOS technology. Digital integrated circuits based on this technology were first introduced by RCA as the CD4000 series, which is now also available from several other manufacturers. While normally the acronym CMOS is used for the technology, RCA favors the term COS/MOS. Another family of CMOS ICs is the 74C series, which is pin compatible with the well-known 7400/5400 TTL series. Until not too long ago, CMOS ICs were a rarity on the surplus market and, if available, were much more expensive than comparable TTL ICs. But today CMOS ICs are available from many mail order suppliers. While prices have come down substantially, they still can differ a lot between dealers and it pays to compare advertisements. Because the CD4000 series seems to be available more readily than the 74C series, it was used in the design of the MINI-MOS keyer.

The operation of the keyer circuit will be described using the "positive logic" convention. This simply means that when the voltage at a certain point in the circuit is "high" (close to the positive supply voltage VDD), it will be assigned a logical "1." Conversely, the logical "0" corresponds to a "low" voltage (close to the negative supply voltage VSS).

Fig. 2 shows the circuit diagram of the keyer and lists the parts used. The dot and dash contacts of the keyer paddles are connected to two RS (reset-set) flip flops which serve as memories for the entered code elements. These flip flops are made up from four NAND gates contained in IC U1. One of the flip flops is redrawn in Fig. 3, which also shows the so-called "truth table" of the circuit. This table simply indicates the voltages at the outputs Q and $\overline{Q}$ of the circuit for the four possible combinations of input voltages. While these flip flops store the entered dot or dash, the code element currently being sent is stored in one of the two flip flops U3A and U3B. These flip flops are of the D (data) type and can be set and reset in two different ways. A logical 1 at the S or R input of the flip flop will set or reset it asynchronously – that is, at the instant the voltage goes from low to high. The flip flop can also be set by a logical 1 and reset by a logical 0 applied to the D input. This, however, occurs synchronously with a clock signal applied to the C (clock) input and at the instant this signal makes a transition from high to low.

When the keyer is in standby (that means if no code element is currently being sent), dot flip flop U3A as well as dash flip flop U3B are in the reset position and both their $\overline{Q}$s will be high. In this case the output of AND gate U4A is also high. This output is connected to one input of the AND gates U2B and U2D. This has the effect that the output of the dot memory is connected to the S input of dot flip flop U3A, while the output of the dash memory is connected to the S input of dash memory U3B. One input of NOR gate U7A also receives a high signal which stops the clock.

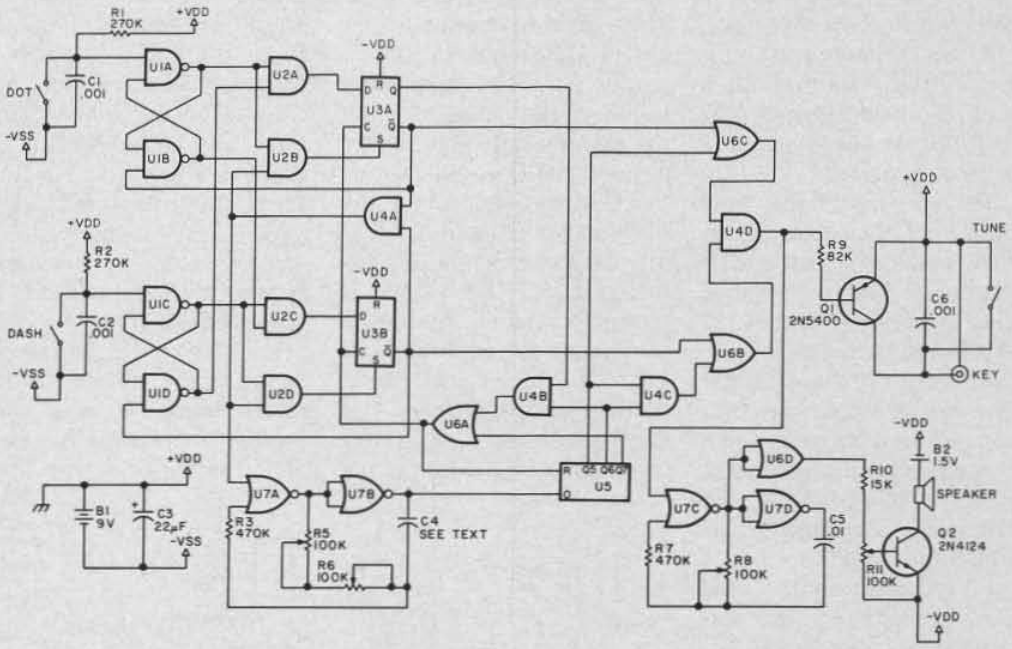
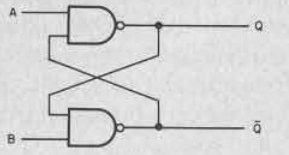


Fig. 2. Circuit diagram of the MINI-MOS keyer. Parts list: U1 – 4011 quadruple 2-input NAND; U2, U4 – 4081 quadruple 2-input AND; U3 – 4013 dual D-type flip flop; U5 – 4024 7-stage binary counter; U6 – 4071 quadruple 2-input OR; U7 – 4001 quadruple 2-input NOR; Q1 – 2N5400 or other small signal PNP transistor with a voltage rating sufficient for the keying voltage of the transmitter; Q2 – 2N4142 or most any other small signal NPN silicon transistor; R5, R11 – miniature potentiometers, 100k Ohm linear taper; R6, R8 – trimpots, one turn, 100k Ohm; C4 – see text; C3 – 22 microfarad, 15 volts; B1 – standard 9 volt transistor battery; B2 – AA cell, regular or alkaline type; SP – miniature speaker, 2 inch diameter (Radio Shack or other).

Fig. 3. Reset-set (RS) type flip flop made up from NAND gates. The "truth table" shows the relation between signals at the inputs and outputs of the circuit.



	A	B	Q	$\bar{Q}$
SET	0	1	1	0
RESET	1	0	0	1
STORE	1	1	X	$\bar{X}$
AMBIGUOUS	0	0	1	1

Now, when either the dot or the dash contact is closed, causing a logical 0 at the set input of the dot or dash memory, the Q output of this memory flip flop will go high. This in turn causes the corresponding D flip flop to be set instantaneously via its S input. When the D flip flop is set, its $\bar{Q}$ output goes low. This causes the appropriate memory flip flop to be reset at the instant the dot or dash contact is opened again. The logical 0 at the $\bar{Q}$ output of the D flip flop, via AND gate U4A, also disconnects both memory flip flops from the S input of their associated D flip flop. At the same time the clock is started.

The D flip flops now operate in the synchronous mode and can change their state only when a negative going transition occurs at their C inputs. Let us assume that the dot flip flop U3A has been set in this way, and examine what happens when a negative transition occurs at the C inputs of U3A and U3B. There are actually four different possibilities:

1. The dot contact has been opened and the dot memory has been reset. The dash memory has not been set. This results in a low signal at the D input of U3A. When the clock signal goes low, this flip flop will therefore be reset and the circuit returns to the standby status.

2. The dot contact is still closed and the dot memory, therefore, has not been reset. This causes a high signal at the D input of U3A. This flip flop thus does not change its state when the clock signal goes low, which results in another dot being sent.

3. The dot contact has been opened and the dot memory has been reset, but the dash contact has been closed, setting the dash memory. This results in a low signal at the D input of U3A and a high signal at the D input of U3B. When the clock signal goes low, U3B will be set, while simultaneously U3A is reset. Thus a dash will be sent following the dot.

4. Both the dot and the dash contact are closed and both memory flip flops are therefore in the set position. This would place a logical 1 at the D inputs of both U3A and U3B, were it not for the iambic gates U2A and U2C. These gates have one of their inputs connected to the $\bar{Q}$ output of the "opposite" memory flip flop. Because the dash memory is in the set position, its $\bar{Q}$ output is low. Via U2A this results in a low signal at the D input of U3A. The dot memory is also in the set position, but U3A is trying to reset it. As can be seen from the truth table in Fig. 3, this causes both outputs of the memory flip flop to go high. Via U2C this results in a high signal at the D input of U3B. When the clock signal goes low, this causes U3A to be reset and U3B to be set. If the dot and dash contacts continue to be closed, the process will be reversed the next time the clock signal goes low. The keyer, therefore, will send dots and dashes alternately in the so-called iambic mode until one or both key contacts are opened. (The word iambic, incidentally, comes from the iamb or iambus, a Greek verse in which long and short syllables alternate.)

U3A remains in the set position while a dot is being sent, as well as for the space that follows. The clock pulse to reset U3A, therefore, has to occur two dot elements after the flip flop has been set. The clock pulse for resetting the dash flip flop U3B has to come 4 dot elements after it has been set. In order to obtain the spaces after the dot and dash, pulses after 1 and after 3 dot elements are also required. These pulses are obtained from the clock through a pulse divider. The clock consists of the NAND gates U7A and U7B, which are connected as a free running, gated multivibrator[2,3]. This circuit is amazingly stable, and a variation of the supply voltage between 6 and 10 volts causes a frequency shift of only about 1%. The square wave at the output of the multivibrator is not completely symmetrical, however, and the first period after being gated on may have a slightly different length than the following periods. In order to avoid timing errors, the clock signal was not used directly, but was divided in a frequency divider. The IC U5 very conveniently contains not fewer than seven flip flops which are connected as a seven stage binary counter. The output of the fifth stage, Q5, goes high after 2^4 or 16 input pulses, and goes low again after 2^5 or 32 input pulses. This output is used to represent one dot element. Similarly, the output of the sixth binary stage, Q6, represents two dot elements, and the output of the seventh stage, Q7, four dot elements. A signal representing three dot elements is obtained by connecting Q5 and Q6 to the inputs of AND gate U4C. A reset pulse after 2 dot elements must occur only if a dot is being sent, that is, if U3A is in the set position. Output Q of U3A is therefore used to gate output Q6 via AND gate U4B. If U3A is not in the set position, the reset pulse comes from output Q7 and occurs after 4 dot elements. OR gate U6A is used to combine the two reset pulses. The output of this gate not only provides the clock pulse for the two D flip flops, but also resets the binary counting stages of U5. As a matter of fact, when Q6 or Q7 goes high and applies a high signal to the R input of U5, resetting the binary stages causes the output to immediately go low again. The clock pulse, therefore, is only about one microsecond long.

Most modern transmitters and transceivers use grid block keying and their keying input carries a negative voltage of somewhere between 50 and 150 volts with respect to ground. On "key down," the key has to sink a current of a few milliamperes. This voltage can easily be keyed with a PNP

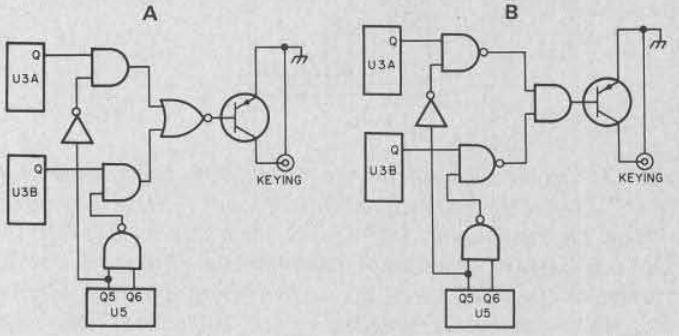


Fig. 4. a. First design of the keying section. b. DeMorgan's theorem (see text) applied to the NOR gate.

FIRST

Make this comparison:

The GTX-1 gives the high quality performance that compares with Motorola, GE, RCA or any other hand-helds that sell for $700 or more.

THEN

Check these features:

Small: only 8"x2.6"x1.28" . . . **Appearance:** slim silhouette all black metal . . . **Serviceable:** easy access to separate receive and transmit circuit boards . . . **PLUS:** 6 pole xtal filter for superlative receiver operation . . . **and:** trimmers on receive and transmit xtals: standard 10.7 MHz 1st IF.

and specs:

Rec. Sens.: .2μv for 12 db SINAD . . . **Adjacent channel rejection:** ±30 kHz 55 db . . . **Spur. Resp.:** more than 65 db . . . **Audio Output:** 500 mw . . . **Power output:** Hi 3 w, Lo 1 w . . . **Audio Quality:** Distortion free, crisp, clear receive and transmit.

NOW

Look at the Price:

GTX-1
2 Meter 6 channel Hand-Held (without encoder)
$249.95
(Bat. Not Incl.)

GTX-1T
with Built-In Tone Encoder
$299.95
(Bat. Not Incl.)

GENAVE stocks most common 2-M Xtals for immediate delivery

Genave

Use This Handy Order Form

4141 Kingman Dr., Indianapolis, IN 46226
Phone-in orders accepted (317+546-1111)

☐ **GTX-200-T**
2-meter FM, 100 channel combinations, 30 watts with factory installed tone encoder (Incl. 146.94 MHz)

$249.95

☐ **GTX-200**
2-meter FM, 100 channel combinations, 30 watts (Incl. 146.94 MHz)

$199.95

☐ **GTX-10-S**
2-meter FM, 10 channels, 10 watts (Xtals not included)

$149.95

☐ **GTX-2**
2-meter FM, 10 channels, 30 watts with pushbutton frequency selector (Incl. 146.94 MHz)

$189.95

☐ **GTX-I**
2-meter FM, 6-channel, 3.5 watts Hand-Held
$249.95
(Bat. not incl.)

☐ **GTX-IT**
Same as GTX-1, plus Factory Installed Tone Encoder
Operate Auto Patch
$299.95
(Bat. not incl.)

☐ **Ringo Ranger ARX-2 6 db 2-M Base Antenna** @ $29.95 $_____

☐ **Lambda/4 2-M and 6-M Trunk Antenna** @ $29.95 $_____

☐ **TE-I Tone Encoder Pad** for plug-in installation on most amateur transceivers @ $59.95 $_____

☐ **TE-II Tone Encoder Pad** for installation on most Hand-Helds @ $49.95 $_____

☐ **PS-1 AC Power Supply** for use with all makes of transceivers 14 VDC-6 amps @ $69.95 $_____

and the following **standard** crystals @ $4.50 each $_____
Non-standard crystals @ $6.50 each: ..... $_____

ACCESSORIES FOR GTX-1 and GTX-1T

☐ **PSI-18** Optional Nicad battery pack $29.95 $_____

☐ **PS-2** Charger for GTX-1(T) battery pack $39.95 $_____

☐ **GLC-1** Leather carrying case .....$12.95 $_____

☐ **TE-III** Tone Encoder (for use with GTX-1) $49.95 $_____

Add $4 per Radio for Shipping, Handling, and Crystal Netting.

Payment by:
☐ Certified Check/Money Order ☐ Personal Check
☐ C.O.D. Include 20% Down

Note: Orders accompanied by personal checks will require about two weeks to process.
20% Down Payment Enclosed. Charge Balance To:

☐ BankAmericard #_____ Expires _____
☐ Master Charge #_____ Expires _____
☐ Interbank #_____ Expires _____

IN residents add 4% sales tax:
CA residents add 6% sales tax: $_____

All orders shipped post-paid within continental U.S.
(allow 8 weeks delivery.)

NAME _____

ADDRESS _____ CITY _____

STATE & ZIP _____ AMATEUR CALL _____

8 7 6

CLIP OUT AND ORDER NOW — CLIP OUT AND ORDER NOW

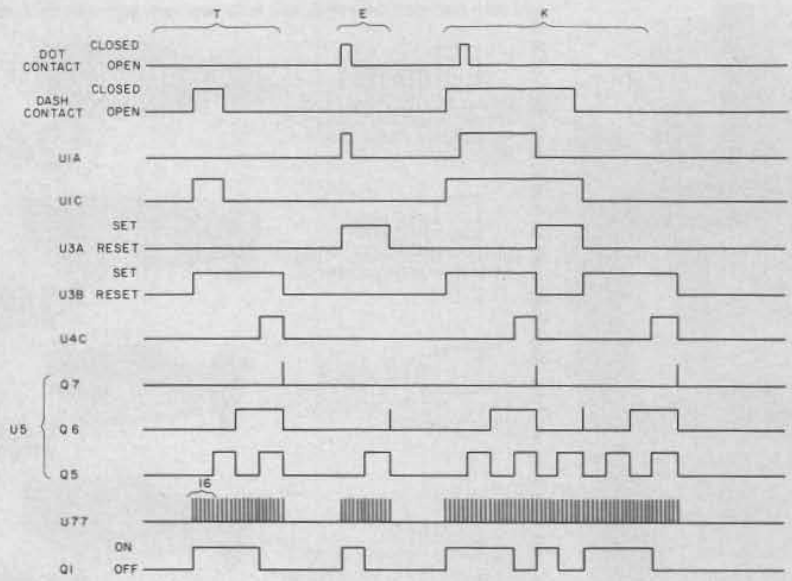


Fig. 5. Pulse diagram showing the signals at different points of the circuit when the letters "-T-E-K-" are being sent.

transistor of sufficiently high voltage rating. The emitter of this transistor has to be connected to the +VDD voltage of the CMOS circuit. The transistor is turned on by a logical 0 at its base.

The initial design of the keying section is shown in Fig. 4a. The two AND gates together with the inverter and NAND gate are used to turn the keying signal off during the last dot element of a keying cycle, thus providing the space after the dot or dash. The circuit in this form, however, does not utilize efficiently the gates that are left over from the timing section of the keyer. The circuit of Fig. 4a was therefore modified using a rule known as the DeMorgan theorem (named after a 19th century British mathematician). This rule simply states that a gate can be replaced by its opposite type (AND with OR or OR with AND) if inputs and output of the gate are inverted. If this rule is applied to the NOR gate of Fig. 4a, the circuit of Fig. 4b is obtained. If the rule is applied a second time, this time to the two NAND gates of Fig. 4b, the final circuit shown in Fig. 2 results, which utilizes the available gates much more efficiently than the initial design.

The sidetone oscillator was built from the remaining two NOR gates (U7C and U7D), using the same circuit as for the clock. One OR gate, U6D, which was left over, was put to good use as a buffer to make the frequency of the sidetone oscillator independent of the sidetone volume. U6D has to be connected to the output of U7C, which is low during standby to keep current from flowing during the standby mode. The sidetone signal is applied to the base of transistor Q2, which is driven in class C mode. When volume control R11 is completely counterclockwise, Q2 remains cut off and no separate on-off switch for the sidetone is necessary. The power for the speaker is supplied by a separate battery (one AA cell). This was found to be simpler than providing an output transformer for the speaker.

The keying transistor, Q1, is rated for a maximum collector-emitter voltage of -120 volts. Its current sinking capability is determined by the resistance of R9. With the value given in Fig. 2, the keyer can sink currents of up to 4 milliamperes even when the battery voltage has dropped to 6 volts.

For use with a cathode- or emitter-keyed transmitter, Q1 can be used to drive an NPN transistor with a voltage and current rating sufficient to key the transmitter. In this case R9 has to be chosen so that the NPN transistor saturates safely on "key down." The MINI-MOS keyer also will have to be grounded at the -VSS rather than the +VDD side of the battery. This modification, however, is likely to increase the current drain on the battery.

In order to show how the different parts of the MINI-MOS keyer circuit work together, a timing diagram is given in Fig. 5. This diagram shows the voltages at various points of the circuit when the letters "-T-E-K-" are being sent. For the letter K, which has been shown as being sent in the iambic mode, the function of the dot and dash memories can easily be seen.

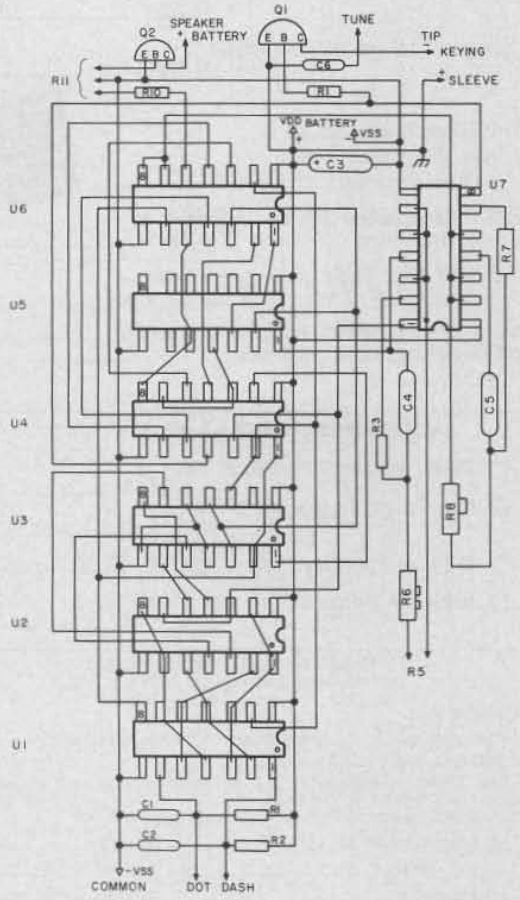


Fig. 6. Wiring diagram of the MINI-MOS keyer. View is at the pins *of the integrated circuits.*

Construction of the Keyer

It is much easier to build the MINI-MOS keyer than to

understand the functioning of its circuit. The circuit was assembled on a small piece of perforated circuit board. The wiring was done with #24 bus wire, using spaghetti tubing (preferably teflon) as insulation at the points of wire crossing. All that is necessary for this technique is a small soldering iron, tweezers, a steady hand, and — if one is over 40 — a good watchmaker loupe. Long wire runs, like the supply buses, were "woven" through the holes of the circuit board to stabilize the wire in order to prevent shorts. From previous experience, however, it was found advisable to work from a wiring diagram in order to prevent errors. This wiring diagram is shown in Fig. 6. (It would be a service to mankind if some fellow ham experienced in the fine art of PCB layout would convert Fig. 6 into a printed circuit board.) A view of the completed circuit board, mounted in the minibox together with the other components, is shown in Fig. 7.

It might be worth mentioning that the circuit was first assembled on one of the plug-in boards available for the breadboarding of IC circuits. In transferring the breadboard to the final circuit board, an unusual problem was encountered: The circuit did not work, because the pinout diagram for the CD4013 in the RCA databook (1975 edition) contained an error (Fig. 6, however, shows the correct connection).

The keyer has only three external controls: adjustments for code speed (R5) and sidetone volume (R11), and the tuning button, which was mounted on top of the minibox. Trimpots, accessible through holes, allow setting of the sidetone frequency (R8) and the maximum code speed (R6). The minimum code speed is determined by C4. When a .05 microfarad capacitor is used, the slowest code speed is about 5 wpm, while a .025 microfarad capacitor results in a minimum speed of about 10 wpm. These capacitors should be of the mylar type in order to avoid frequency changes with changing temperatures. Because of the stability of the clock circuit, it is actually possible to calibrate R5 directly in wpm, which should be of interest if the keyer is used to send code practice lessons. The standard code speed, as it is used for the FCC code test, is based on words exactly 50 dot elements long (the reference word is "Paris"). Because 16 pulses at the output of the master clock (U7B) correspond to one dot element, the code speed can be calibrated by measuring the clock frequency. If available, a counter can be used for this purpose; otherwise, the frequency can be beat against an audio oscillator. A code speed of "X" wpm corresponds to a clock frequency of X times 13.3 Hz. Thus a code speed of, for instance 20 wpm, is sent when the clock is set to a frequency of 266 Hz.

The standby current drawn by the circuit is less than 1 microampere. In the standby mode the life of the battery, therefore, is actually determined by its shelf life. On "key down" (actually, when both paddles are pressed), the circuit draws between 850 and 1000 microamperes, depending on the setting of the sidetone volume. For this current value the tables of the battery manufacturers show an estimated life of about 450 hours until the battery has been discharged to 5 volts. The battery should therefore be good for well over one year of daily operation. So, once a year let the MINI-MOS keyer have a new set of batteries, whether it needs it or not. The sidetone amplifier, however, at maximum volume draws up to 10 milliamperes of current. With a standard (carbon-zinc) AA cell, this results in a battery life of only about 200 operating hours. If the sidetone is used at high volume settings, use of an alkaline type AA cell is therefore recommended to assure a full year of operation on one set of batteries.

The MINI-MOS keyer can be operated with any single or double (squeeze) paddle key, although the iambic feature can, of course, be utilized only with the latter type. ■

References

[1] James W. Pollock WB2DFA, "COSMOS IC Electronic Keyer," *Ham Radio*, June 1974, page 6.

[2] J. A. Dean and J. P. Rupley, "Astable and Monostable Oscillators using RCA COS/MOS Digital Integrated Circuits," *RCA Application Note ICAN-6267.* (This application note is reprinted in the RCA COS/MOS data book, 1974 and 1975 editions.)

[3] *RCA COS/MOS Integrated Circuits Manual,* Technical series CMS 271, page 89.

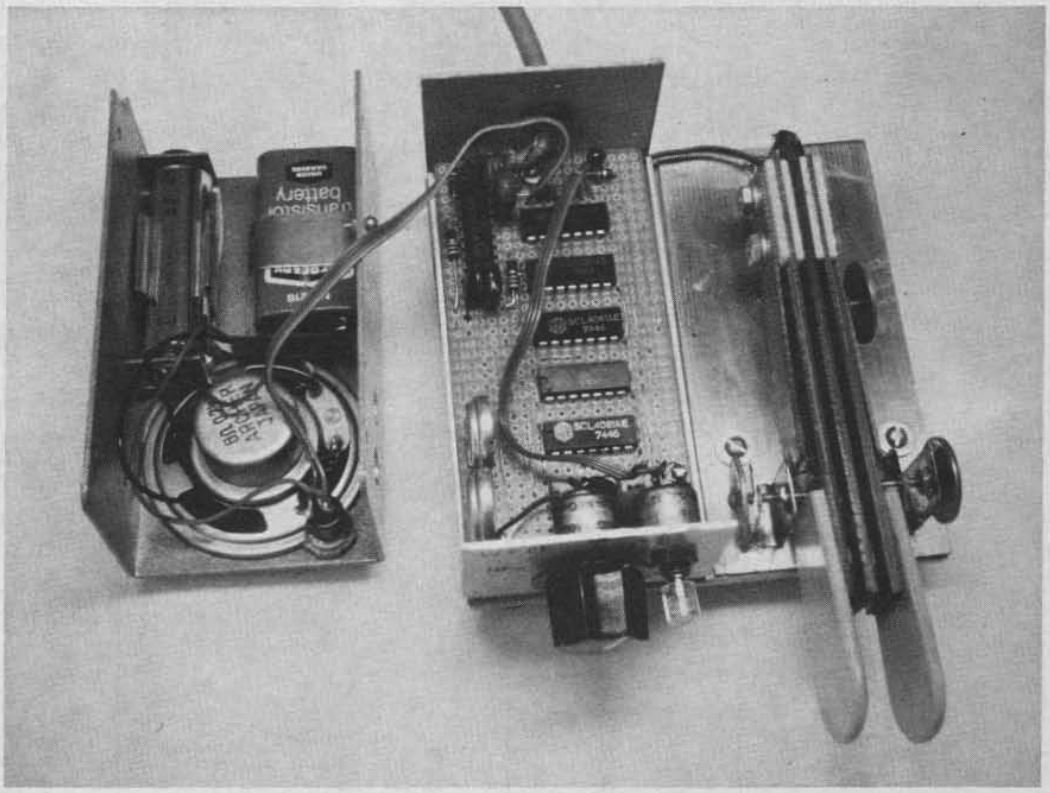


Fig. 7. View of the completed keyer with the top of the minibox removed. The sidetone speaker, the batteries and the tuning push-button are mounted in the top and connected to the circuit board by a 4 lead ribbon cable.